Reconfigurable Computing Using FPGA: State of the Art and Potential for Systolic Array Applications

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1. Introduction

Our research group is investigating the use of systolic array processors based on multi FPGA (field-programmable gate array) technology to accelerate computational tasks in computation intensive algorithms. In this paper, we investigate first the state-of-the-art reconfigurable computing. We first define the implementation spectrum, classify and characterize the different level of abstraction (logic, functional and system). Then, we review in detail the basic building blocks of reconfigurable devices, essentially, the field-programmable gate arrays (FPGAs). As a final step, we look for potential multi-FPGA systems and their interconnections in systolic array applications.

2. Content

Fig. 1 shows the implementation spectrum in reconfigurable computing [1]. The spectrum is bounded by three axes symbolising the performance, flexibility and cost. The figure clearly shows that ASIC gives high performance at the cost of inflexibility, processor is very flexible but not tuned to the application and that RC hardware is a nice compromise.

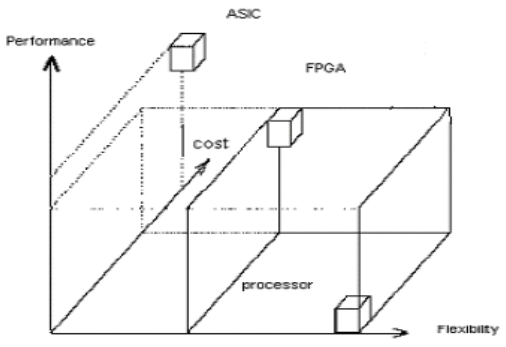

Fig.1: Implementation Spectrum.

Reconfigurable hardware can be classified according to their granularity level, which are: the system level, the functional level and the logic level; and their type of reconfiguration (Static, semi-static and dynamic). There are two basic categories of FPGAs in the market today: SRAM-based FPGAs and antifuse-based FPGAs. Modern VLSI FPGA architecture shown in Fig. 2 is characterized by the integration of different building blocks [2] such as:

- Logic cell (Combinational and Sequential);
- Dedicated Arithmetic Logic, processors; and
- Input/Ouput, JTAG, Gigabits transceiver blocks.

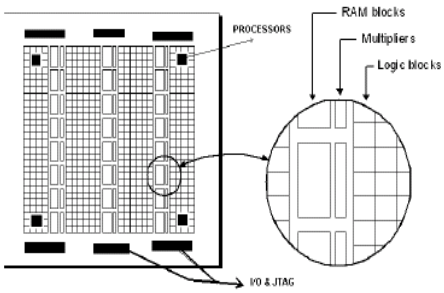

Fig.2: FPGA with embedded system functionality.

Today's high-end FPGAs such as the VIRTEX-II PRO, VIRTEX4 and VIRTEX5 from XILINX include special hard-wired gigabit transceiver blocks [3]. These blocks use one pair of differential signals to transmit data (TX) and another pair to receive data (RX). These transceivers operate at very high speeds (up to 10 Gbps), allowing them to transmit and receive serially billions of bits of data per second. If a network of FPGAs makes up the system, then each may execute an individual process and communications are carried out directly via explicit FPGA to FPGA channel. The same machine instruction is used whether a single FPGA or many are being used as in the SIMD computer architecture.

One such implementation in multi-FPGA systems and their interconnections is the systolic array. By analogy with the regular pumping of blood by the heart, a systolic array is an

arrangement of processors in an array (often rectangular) where data flows synchronously across the array between neighbours, usually with different data flowing in different directions. H. T. Kung and Charles Leiserson publish the first paper describing systolic arrays in 1978 [4]. Each processor at each step takes in data from one or more neighbours (e.g. North and West), processes it and, in the next step, outputs results in the opposite direction (South and East). The following are reasons why an FPGA is suited for systolic array applications:

- FPGA has many LUTs and multipliers. Therefore, it is better suited for parallel operations.
- FPGA is high performance. It easily allows time division multiplexing for slower data rates, and so can accommodate multiple channels running simultaneously.
- FPGA cost is coming down and close to the cost of ASIC or DSP processor solutions.

3. Conclusion

Our study shows inter-chip connectivity as an issue in using gigabit transceivers for High speed FPGA-FPGA connections to make multiple FPGAs more like one big FPGA and the suitability for spatially parallel applications using systolic arrays.

References

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[2] The Design Worrior's Guide to FPGAs Devices, Tools, and Flows. ISBN 0750676043, Mentor Graphics Corp. (2004).

[3] Amit Dhir and Delfin Rodillas, Programmable Logic Solutions for Next Generation Serial Backplanes, Xilinx white paper, http://www.xilinx.com/esp/backplanes.

[4] H. T Kung and C. E. Leiserson, Systolic Array for VLSI, Sparse Matrix Proc. (1979) p. 256.