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Power-Grid Load Balancing by Using Smart Home Appliances

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***Abstract*—Climate change is one of the greatest environmental, social and economic threats facing the planet, and can be mitigated by increasing the efficiency of the electric power generation and distribution system. Dynamic demand control is a low-cost technology that fosters better load balancing of the electricity grid, and thus enable savings on CO_2 emissions at power plants. This paper discusses a practical and inexpensive solution for the implementation of dynamic demand control, based on a dedicated peripheral for a general-purpose microcontroller. Pre-production test of the peripheral has been carried out by emulating the actual microprocessor. Simulations have been carried out, to investigate actual efficacy of the proposed approach.**

I. Introduction

Global warming is a major concern nowadays, mostly due to the increase on greenhouse gases concentration in the atmosphere. Power plants burning fossil fuel are responsible for a significant fraction of greenhouse pollutants emission. Among many issues, the global efficiency of power grid is limited by the need of providing a sufficient amount of spare power to face unpredictable demand peaks. Renewable energy sources (wind, solar plants) cause much lower pollution, but provide an inherently intermittent supply, thus again resulting in grid balancing issues. Erratic load imbalances are compensated, at the *supply-side*, by a service called "response", which involves the use of spare generators. Such generators usually operate at low-output regimes to provide back-up capacity, and their efficiency is lower than at full-power regimes. This relatively increases the greenhouse gas emissions. Consequently, there is a growing interest for *demand-side* techniques which, by adapting the user's load to the grid actual availability, would help in smoothing out fluctuations in the power requirement.

Dynamic Demand Control (DDC) technology [1] has been proposed in late '70s [2, 3] as a solution directed to reduce costs of electric power. It aims at a better matching between power supply and demand by exploiting self-balancing capability on the load's end, rather than relying on statistical prediction on the power-grid end. Recently, the DDC approach has been retrieved: energy authorities are interested in incentivating DDC technology and UK Government has recently supported a large-scale field-trial [1]. Nevertheless, cheap devices are needed to support massive deployments: in this abstract, a device conceived for low-cost DDC implementation in home digital appliances is presented.

II. Dynamic Demand Control

DDC is sensitive to the mains frequency. Power grid operators have to keep the frequency within strict limits (e.g. $f_{mains} = 50 \pm 0.5$ Hz in several European countries). In practice, the frequency normally remains within even stricter bounds

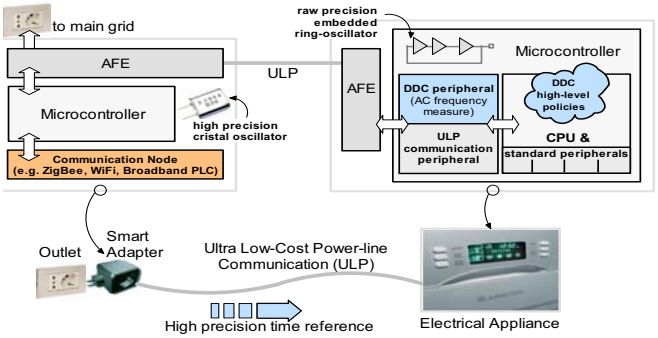

Fig. 1. DDC/ULP peripheral structure and connectivity.

(± 0.2 Hz) but changes on a short time basis (minutes or even seconds). A frequency decrease can be correlated to an increase of the grid load [2], so that a frequency monitor could be exploited to evaluate the stress status of the grid.

At the user's side, such an information can be used to decide whether inserting a load or waiting for an healthier grid status: a wide variety of home appliances may indeed tolerate moderate time shifts in their operating cycle without compromising their function (e.g., heaters, air conditioners, fridges, freezers, etc.). DDC allows the load to re-schedule its power request, according to the actual power-grid availability. If a large number of DDC-enabled device were connected, this would result in a self-balancing capability of the global network, ensuring a more stable cumulative load and thus reducing the need for spinning reserves.

III. Hardware Architecture

Although software implementation of DDC-related algorithm is not difficult at all, it may require significant amount of software resources, not necessarily affordable in the tight economic constraints of home appliances market. In our work we decided to implement dedicated hardware to provide basic frequency monitoring functions, letting the software layer take care of comparison and decision policies. In [4, 5] the implementation of a microcontroller peripheral has been described, aimed at allowing white goods network connectivity (Ultra Low-cost Powerline, ULP communication). Here, we exploit a similar concept, adding DDC functionality to the same framework and sharing common subsystems (e.g. analog interfaces). The overall network structure is shown in Fig. 1: the microcontroller communicates with the power grid through an inexpensive analog front-end (AFE), which provides the digital controller with power supply waveform sampled data.

A zero-crossing signal (ZC_1) can be used to evaluate actual AC frequency: binary counters are integrated in the circuit, suitable for the required frequency resolution; frequency can be averaged over a programmable interval (ranging from 2^1 to 2^8 cycles) and a configurable-threshold comparator allows for

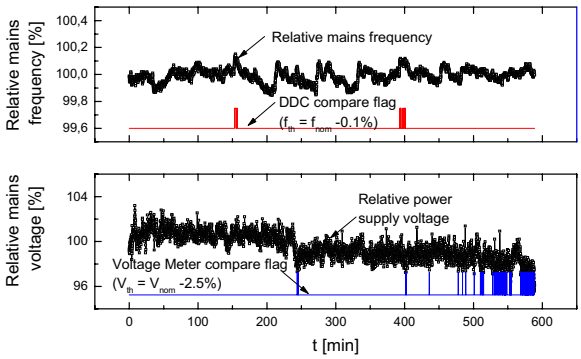

Fig. 2. Sample power-supply frequency and voltage log.

estimating actual deviation from the reference value. Both configuration data are passed through the peripheral register interface. By exploiting a second waveform sample (ZC_2), the actual wave amplitude can be estimated as well. A key issue concerns the measurement quality: discriminating DDC intervention thresholds require some 0.1 % precision and accuracy. However, time reference is given by the digital-domain clock, which is usually based on coarse ring oscillators, to avoid expensive crystal resonators. Depending on the microcontroller main clock frequency (2÷30 MHz), peripheral clock spans from 1 to 1.875 MHz, enabling for at least 0.005% precision in period fluctuation detection. The internal oscillators design accuracy is typically limited to few percentage points. Calibration is hence needed to attain the required reliability: to this purpose, ULP communication [4] is exploited to connect to an external high-precision reference simply through the power cord. This can be accomplished at the factory, during the assembly-line test, or at home, if a smart-adapter [5] node is exploited for home-networking.

IV. Experimental Results

In cooperation with Renesas Corporation, the circuit has been designed and incorporated into the architecture of a standard microcontroller, and a first test production is under way. To provide pre-production test, we mapped the DDC/ULP peripheral onto an Altera FPGA board, connected to the microprocessor internal busses through a Renesas E6000 real-time, in-circuit emulator. In Fig. 2(a), a sample frequency log is reported, together with the DDC comparator output, with threshold set to 0.1% deviation from the nominal, 50 Hz value.

Similar curves can be obtained from the voltage monitoring section, shown in Fig. 2(b), which can be exploited for early black-out detection. Once basic functionalities have been validated, we simulated the behavior of a home freezer, comparing standard and DDC-controlled performance. We assumed the frequency distribution shown in Fig. 3(a), averaged on 5 sec intervals. In standard operating mode (Fig. 3(b)), the freezer compressor is switched on and off as soon as the internal temperature exceeds an upper and lower limit, respectively, thus keeping the average temperature within a given safe range. We then simulated the DDC intervention, simply by modulating the threshold temperatures

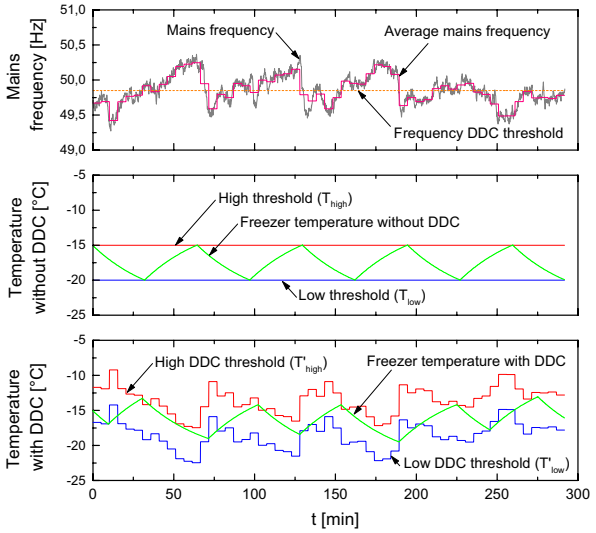

Fig. 3. Application of DDC algorithm.

TABLE I

	Avg. Temp.	Compressor avg. duty cycle	Compressor work during overload
DDC off	-17.57 °C	55.43 %	40.16 %
DDC on	-16.15 °C	51.04 %	14.30 %

according to the actual frequency shift: if the frequency lowers, the maximum allowed temperature is increased (still remaining in the safe area), delaying the actual switch-on of the compressor until power-grid status relaxes or the increased temperature threshold is reached (Fig. 3(c)). Results are summarized in Table I, for a given control data set, and show the DDC effectiveness in reducing significantly the compressor work during overload periods, without compromising the freezer functionality. The average temperature slightly increases, and the actual compressor duty cycle (hence the required power) consequently lowers. This suggests that even the small overheating could be almost compensated by smarter tuning of DDC policies, still without power penalties.

V. Conclusions

In this paper we introduce a new microcontroller peripheral, featuring a hardware frequency monitor and aimed at dynamic demand control implementation. The peripheral embeds further communication and monitoring functions, suitable for the development of "intelligent" appliances. Test and simulations have been carried out to evaluate potential benefits of the DD-controller in balancing the power grid load, possibly contributing to reduce global warming effect.

References

[1] Dynamic Demand Web Site (June 2007). [Online]. Available: http://www.dynamicdemand.co.uk/index.htm

[2] F. C. Schweppe, "Power Systems '2000': hierarchical control strategies", *IEEE Spectrum*, July 1978.

[3] F. C. Schweppe, United States Patent n. 4.317.049, 23 Feb. 1982.

[4] A. Ricci, et. al., "Implementation and test of a power-line communication system for electrical appliances networking," *10th ISPLC*, Mar. 2006.

[5] A. Ricci, et al., "Electrical Appliances Networking: an Ultra-Low Cost Solution based on Power-Line Communication", *25th ICCE*, Jan. 2007.