

SEVEN LEVEL DIODE CLAMPED MULTILEVEL INVERTER

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ABSTRACT

In photovoltaic power systems where a set of series-connected photo voltaic arrays is connected to a conventional two-level inverter, the occurrence of partial shades and/or the mismatching of photo voltaic arrays leads to a reduction of the power generated from its potential maximum. To overcome these problems, the connection of the photo voltaic arrays to a multilevel diode-clamped converter is considered in this paper. A control of pulse width-modulation scheme is used to trigger the gate of the thyristor. The PWM switching technique in Five-level and seven-level diode-clamped multilevel inverter (DCMLI) has been implemented in MATLAB/Simulink software package and total harmonic distortion (THD) is compared.

Keywords: *Diode Clamped Inverter, Multilevel inverter, PWM switching*

1. INTRODUCTION

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [1]. The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. The so-called “multilevel” starts from three levels. A three-level inverter, also known as a “neutral-clamped” inverter, consists of two capacitor voltages in series and uses the center tap as the neutral. Each phase leg of the three-level inverter

has two pairs of switching devices in series. The centre of each device pair is clamped to the neutral through clamping diodes. The waveform obtained from a three-level inverter is a quasi-square wave output if fundamental frequency switching is used [2].

The main multilevel topologies are classified into three categories: diode clamped inverters, flying capacitor inverters, and cascaded inverters. In a three-phase inverter system, the number of main switches of each topology is equal. Comparing with the number of other components, for example, clamping diodes and dc-link capacitors having the same capacity per unit, diode clamped inverters have the least number of capacitors among the three types but require additional clamping diodes. Flying capacitor inverters need the most number of capacitors. But cascaded inverters are considered as having the simplest structure. The diode clamped inverter, particularly the three-level one, has drawn much interest in motor drive applications because it needs only one common voltage source. Also, simple and efficient PWM algorithms have been developed for it, even if it has inherent unbalanced dc-link capacitor voltage problem. However, it would be a limitation to applications beyond four-level diode clamped inverters for the reason of reliability and complexity considering dc-link balancing and the prohibitively high number of clamping diodes [3]. Multilevel PWM has lower dV/dt than that experienced in some two-level PWM drives because switching is between several smaller voltage levels [4].

2. DIODE-CLAMPED MULTILEVEL INVERTER

An m-level diode-clamp inverter typically consists of $m - 1$ capacitors on the dc bus and produces m levels of the Phase voltage. A one

leg of three-phase nine-level diode-clamped inverter is shown in Figure 1. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by eight capacitors into nine levels. The voltage across each capacitor is, and the voltage stress across each

switching device is limited to the safe working level through the clamping diodes. Table 1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage as areference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase

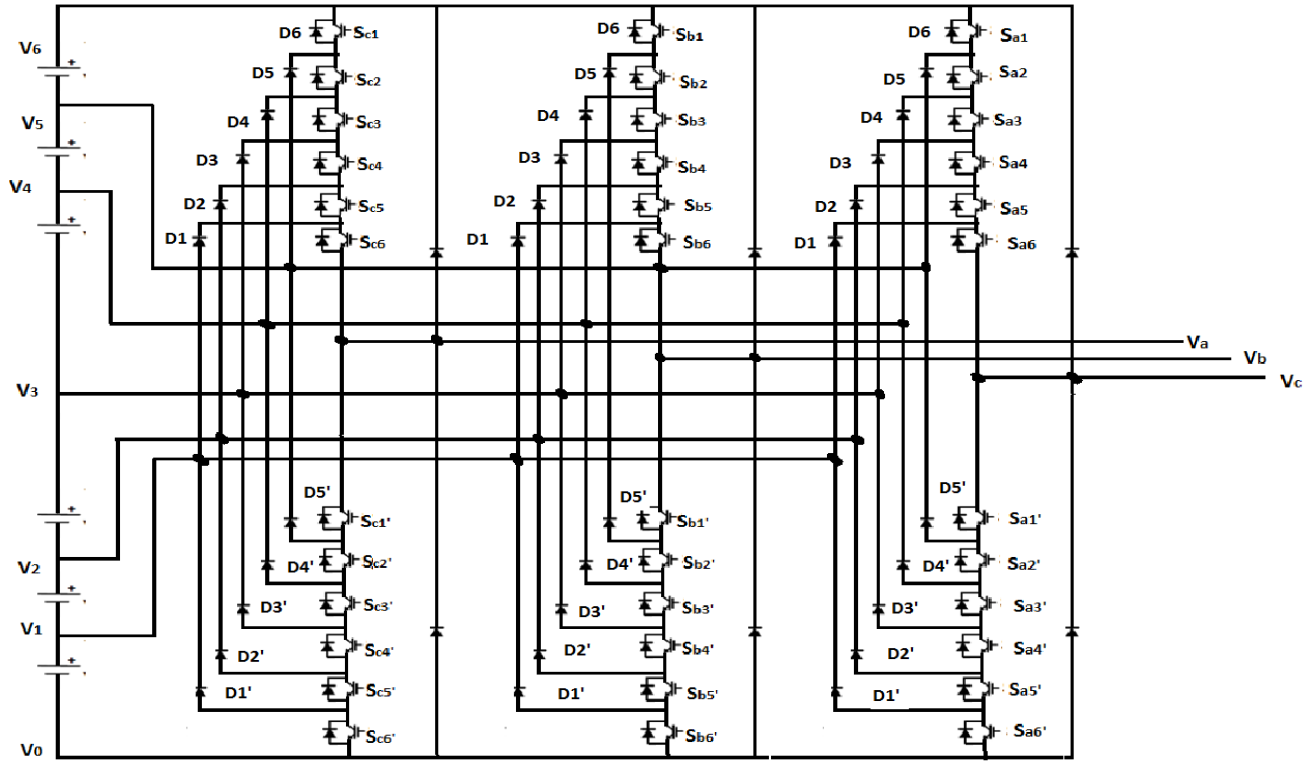


Fig:1 Three phase nine level diode clamped multilevel inverter schematic

VOLTAGE V_a	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	$S_{a1'}$	$S_{a2'}$	$S_{a3'}$	$S_{a4'}$	$S_{a5'}$	$S_{a6'}$
$V_5=5V_{dc}$	1	1	1	1	1	1	1	1	0	0	0	0
$V_4=4V_{dc}$	0	1	1	1	1	1	1	1	1	0	0	0
$V_3=3V_{dc}$	0	0	1	1	1	1	1	1	1	1	0	0
$V_2=2V_{dc}$	0	0	0	1	1	1	1	1	1	1	1	0
$V_1=1V_{dc}$	0	0	0	0	1	1	1	1	1	1	1	1
$V_0=0V_{dc}$	0	0	0	0	0	1	1	1	1	1	1	1

Table:1 DCMLI Voltage Levels and Switching State

has eight complementary switch pairs such that turning on one of the switches of the pair dc V o V require that the other complementary

switch be turned off. The complementary switch pairs for phase leg a are (S_{a1} , $S_{a1'}$), (S_{a2} , $S_{a2'}$), (S_{a3} , $S_{a3'}$) (S_{a4} , $S_{a4'}$) (S_{a5} , $S_{a5'}$) and (S_{a6} ,

Sa6'). Table 1 also shows that in a diode-clamped inverter, the switches that are ON for particular phase legs are always adjacent and in series. For a seven-level inverter, a set of six switches is ON at any given time [5]. Figure 2 shows one of the three line-line output voltage waveforms for a seven-level multilevel inverter. The line voltage V_{ab} consists of a phase-leg a voltage and a phase-leg b voltage. The resulting line voltage is a 7-level staircase waveform. This means that an

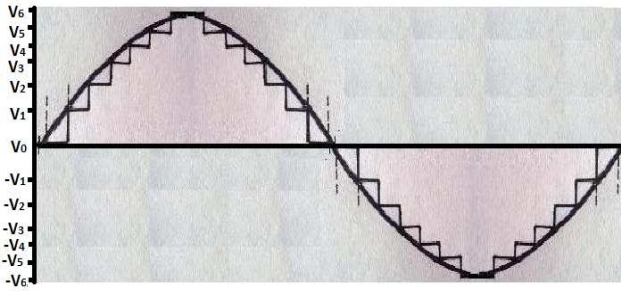


Fig:2 Output line voltage of 7-level DCMLI

m-level diode-clamped inverter has an m-level output phase voltage and a (2m-1)-level output line voltage. Although each active switching device is required to block only a voltage level of dc V , the clamping diodes require different ratings for reverse voltage blocking. Using phase A as an example, when all the lower switches $S_{a1'}$ through $S_{a6'}$ are turned on, D_5 must block five voltage levels, or $5 V_{dc}$. Similarly, D_4 must block 4 dc V , D_3 must block 3 dc V , D_2 must block 2 dc V and D_1 must block 1 dc V . If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, D_n will require n diodes in series; consequently, the number of diodes required for each phase would be $2(m-2)$. Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped inverter. DCMLI has the following advantages and disadvantages.

Advantages:

- (1) DC-link capacitors are common to three phases.
- (2) Switching frequency can be low.
- (3) Reactive current and negative-phase-sequence current can be controlled.

Disadvantages:

- (1) Many diodes are used for clamping.
- (2) Many diodes make physical layout difficult, e.g. increase stray inductance [6].

3. PWM method for Seven-level DCMLI

Pulse width modulation (PWM) strategies used in a conventional inverter can be modified to use in multilevel inverters. Previous authors (McGrath, B.P. and D.G. Holmes) have extended several different two-level multilevel carrier-based PWM techniques as a means for controlling the active devices in a multilevel inverter. The most popular and easiest technique to implement uses several triangle carrier signals and one reference, or modulation, signal per phase.

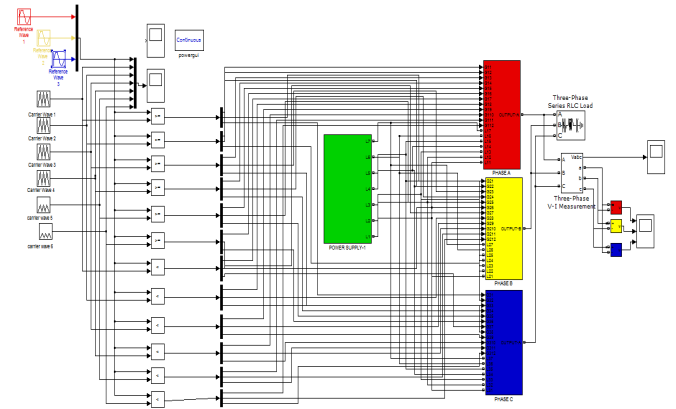


Fig:3 Seven-Level inverter Model

Figure 4 shows the principle of the PWM method for a multilevel inverter. The PWM method generates switching signals by comparing one sinusoidal signal and six triangular wave signals, which have DC bias for each voltage level, as shown in Figure 4. In this modulation method, the duty cycle of each voltage level is determined by the ratio of the sine wave amplitude to the triangular carrier signal amplitude. That is, the sine wave amplitude determines modulation factor, and one modulation factor generates only one pattern of output pulse width [7].



Fig: 4 Sinusoidal PWM

Using PWM modulation explained above, simulations have been conducted to verify the effectiveness of the algorithm. PWM modulation in MATLAB Simulink block diagrams and the nine-level DCMLI is shown in Figure

4. SIMULATION RESULTS

The gate signals of DCMLI power circuits are produced by triangle and sinusoidal comparison in MATLAB/Simulink blocks. The output of five-level and seven-level DCMLI are connected to a load and the voltage waveforms are shown in Figure 5 & 6. In order to get THD level of the waveform, a fast Fourier transform (FFT) is applied to obtain the spectrum of the output voltage, which is shown in Figures 7, 8. The THD of the output voltage of seven-level DCMLI is 10.47%, which shows that lower order harmonics have been eliminated. THD levels of seven level DCMLI and nine level DCMLI are compared in Table 2. From the table, it is clear that the THD value of seven-level DCMLI is lower than that five-level DCMLI.

DCMLI	Five-Level	Seven-Level
THD	16.81%	10.47%

Table:2 THD of seven and nine level DCMLI

The output of 7 level DCMLI is connected to a load and the voltage waveforms are shown in Figure 7&8 are compared. Simulation results reveal that the THD of seven - level DCMLI is less than the five-level DCMLI.

Therefore it is concluded that the THD will be decreased by increasing the level of DCMLI.

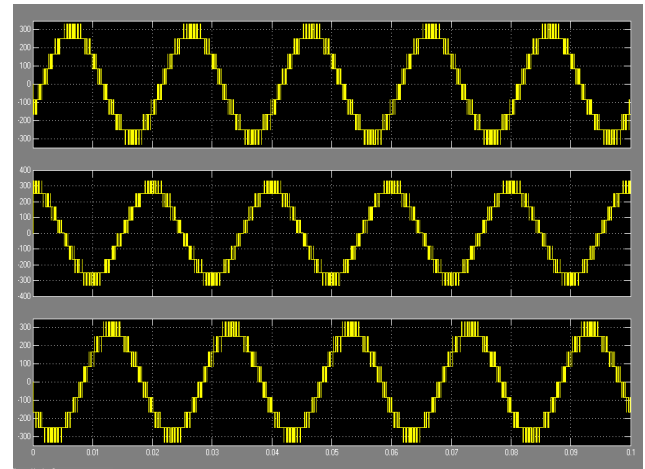


Fig:5 Output of five level DCMLI

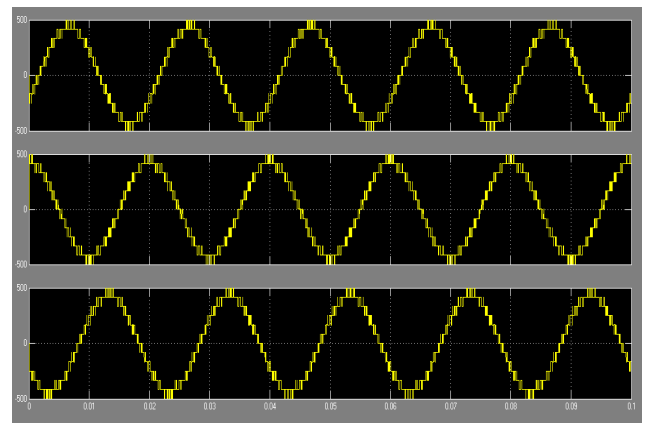


Fig:6 Output of 7-level DCMLI

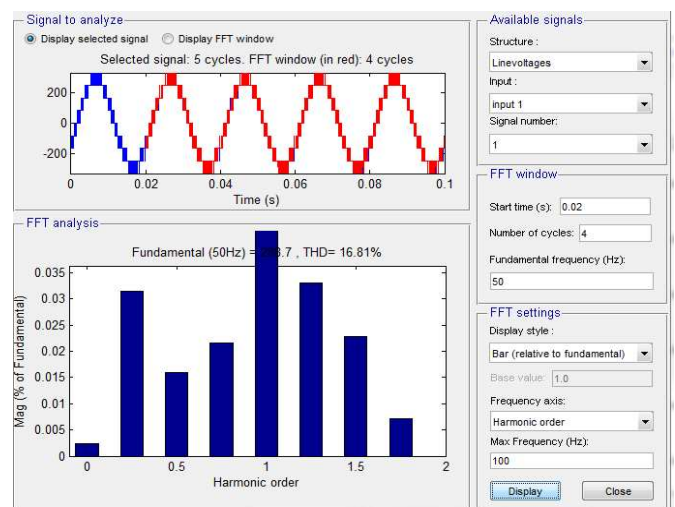


Fig:7 THD of 5- level DCMLI

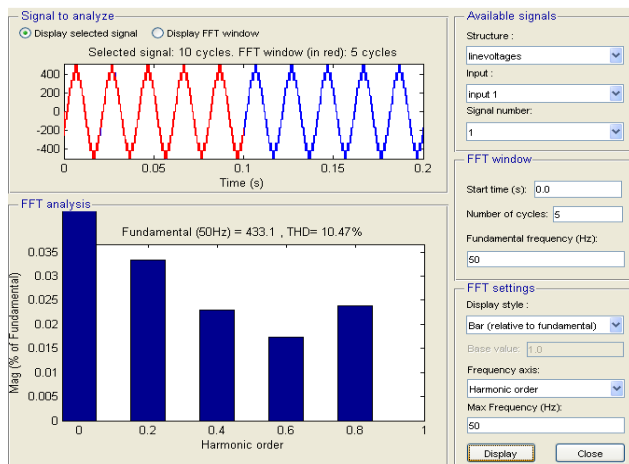


Fig :8 THD of 7- level DCMLI

5. CONCLUSION

In this paper the Five-level and nine-level diode-clamped multilevel inverters for harmonic elimination in MATLAB/ Simulink software package has been presented. The THD levels of Five-level DCMLI and Seven-level DCMLI are compared. Simulation results reveal that the THD of Seven-level DCMLI is less than the Five-level DCMLI. Therefore it is concluded that the THD will be decreased by increasing the level of DCMLI.

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