MINI PROJECT REPORT

TELEPHONE OPERATED

CALLING SYSTEM

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ABSTRACT

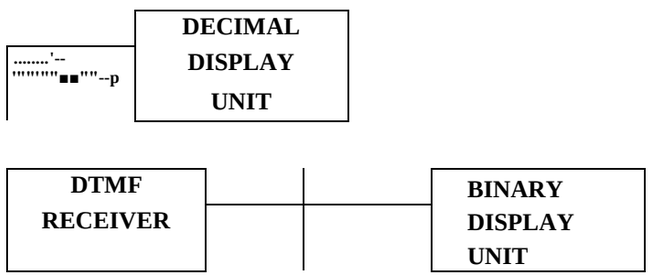
This Telephone Operated Calling circuit is used where persons have to be called or signaled. When you need to call a person amongst many standing outside a cabin, just lift the telephone handset off the cradle and press the respective number. The number of the person called will be displayed and a bell will sound to inform the person that it is his turn. This circuit is very useful for doctors for calling patients, in banks and in various other situations.

CONTENTS

INTRODUCTION

Telephone operated calling circuit converts DTMF signal to its binary equivalent. This circuit consists of a DTMF receiver IC which converts a DTMF input signal in to its binary equivalent. This binary signal is decoded and displayed as its decimal equivalent through the decimal display unit. At the same time it provides a sound alerting signal which informs the people that a number is displayed.

BLOCK DIAGRAM



DTMF RECEIVER

DTMF receiver convert the DTMF signal which is generated at the key pad of the telephone hand set in to its binary equivalent. That is at DTMF receiver a high frequency signal is converted in to its corresponding binary format. The DTMF signals generated by multiplying two signal frequencies which corresponding to the respective row and column frequencies of the signal to be dialed. This frequency is given as DTMF receiver input this signal is converted in the receiver and we obtain the output as the binary equivalent of the dialed number.

DECIMAL DISPLAY UNIT

This unit converted the binary formatted DTMF receiver output to a human readable output. The output from

the DTMF receiver is fed to the binary to seven segment decoder IC which produces the equivalent decoded signal which is then given to the seven segment display.

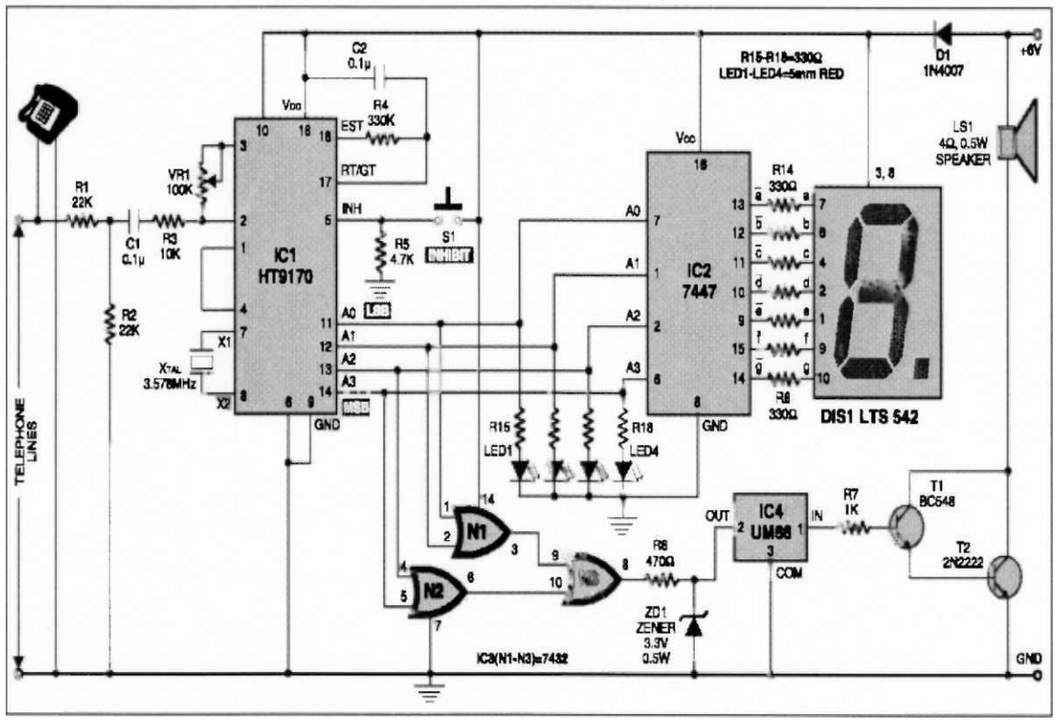
BINARY DISPLAY UNIT

The output of DTMF receiver is also fed to the binary display unit. It is nothing but a combination of 4 LED's. According to the DTMF receiver output the LED glows and hence the binary code is also visible.

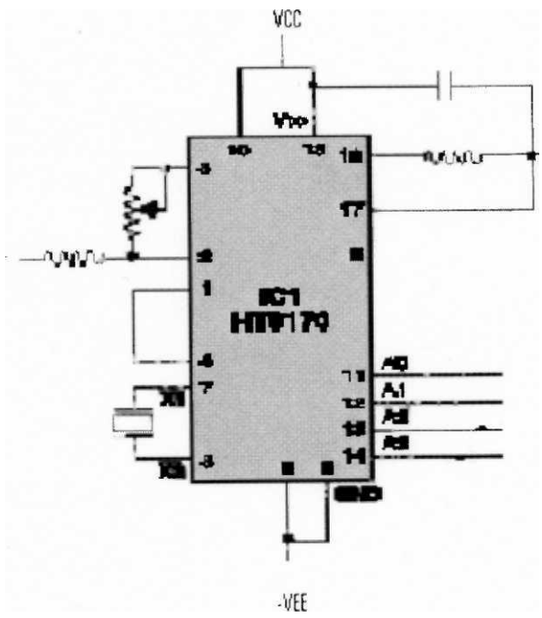
ALERT SOUND UNIT

The output of DTMF receiver is also fed to the alert sound unit. This block provides an alert sound for each binary output. The first stage of alert sound unit is a combination of NAND gate and whose output is high if DTMF receivers show any number. This drives the sound generating IC and here we use UM66 to generate tone. This signal is amplified and is given to the loud speaker.

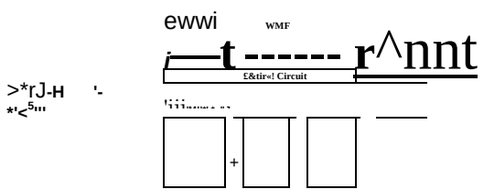
CIRCUIT DIAGRAM



DTMF RECEIVER



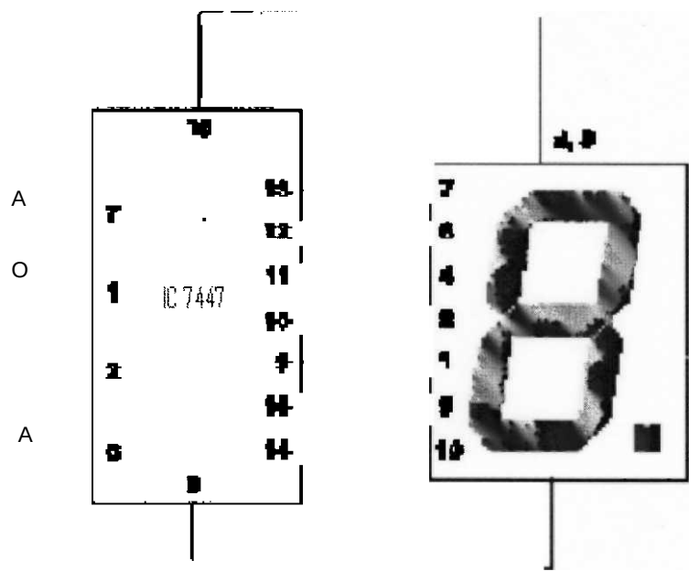
Block Diagram



DTMF receiver converts the DTMF signal in to its corresponding decimal equivalent. A DTMF receiver consists of signal generating section and the signal separating section. The DTMF signal is the multiplication of two signals. The signal separating section converts the single frequency in to two frequencies which are horizontal component and vertical component frequencies. These signals are fed to the decoder section. The decoder converts this signals to their corresponding coded form by compare this frequency to the internally generated signal frequency. This coded form is converted to binary equivalent by the code modulator section. This signal is fed to output.

DECIMAL DISPLAY UNIT

VCC



GNO

In decimal display unit, the output of DTMF receiver is converted into its equivalent 7-segment decimal format. IC 7447 is used for decoding into decimal format. IC7447 is a binary to decimal converter. The output of is given to FND display system. Here the resisters are used to limit the current through the FND.

Vcc=5 Vd=1.5v Id=10mA R =

[Vcc-Vd] /Id R = [5-1.5]/10*10"^{3} R= 350

Q Use 330 Q

BINARY DISPLAY UNIT

AO ^.v^L

Al ---------

A

2

A

3

This section consists of a series combination of resistors and LEDs. The input signal is fed from the DTMF receiver output. According to this signal the LED glows. Here the resistors are used to limit the current through LED.

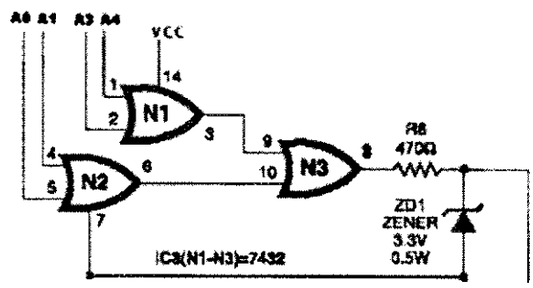
Vcc=5v Ic=15mA

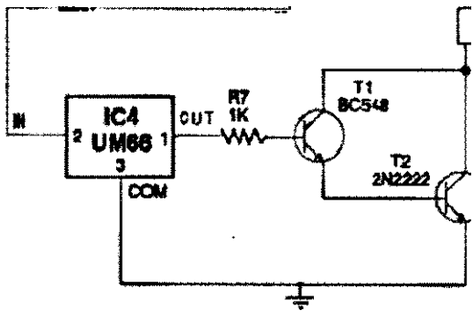
R = Vcc / Ic

R=5v/15mA

R= 330Q

ALERT SOUND UNIT





The output of DTMF is fed to the audio section. It consists of a primary driving circuit and an audio generating section.

The output of DTMF receiver is a binary coded signal. Its value varies from 0000 to 1001. If any of the output is high, the output of the driving circuit is also high. The driving circuit is a combination of NAND gate.

It is connected to UM 66 which is a tone generating IC. According to the output of the driving circuit, UM66 generate the required tone. Transistor T2&T3 get sufficient amplification to the circuit.

To reset the audio section we made the output of DTMF receiver is 0000

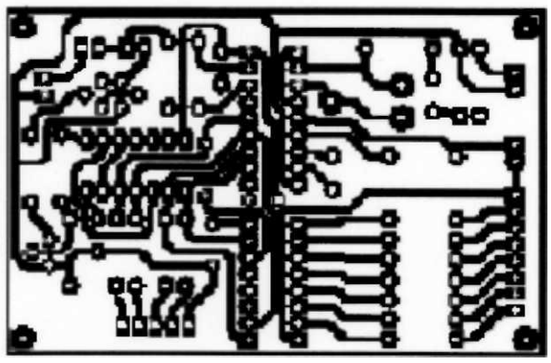
THE PRINTED CIRCUIT BOARD

The first step in assembling is to procure a printed circuit board. The success of a circuit also depends on the PCB. When cost is concerned more than 25% of the total cost is gone for the printed circuit board design and fabrication.

The board is designed using a personal computer. Using the software ORCAD, the layout is drawn. It is then printed on a butter sheet using a laser printer. The layout is transferred to the copper clad sheet using the screen print procedure. First, with the help of a professional screen printer, a negative screen of the layout is prepared. Then the copper clad sheet is kept under this screen. The screen printing ink is poured on the screen as brushed through the top of the screen. For few hours, the printed board is kept under shade till the ink become dry. The etching medium is prepared by mixing anhydrous ferric chloride and water. The printed board is kept in this solution till the exposed copper dissolves in the solution fully. After that the board is taken under a tap and rinsed in flowing water. With the help of a thinner, the ink is removed and the board is coated with solder in order to prevent oxidation.

Another screen which contains component side layout is prepared and the same is printed on the component side of the board. A paper epoxy laminate is used as the board.

PCB LAYOUT



0

-T H11 H

-QP3J-I
U14I-

IC3

I f D

PCB FABRICATION PROCESS

The materials that are used for the fabrication of the pcb are

> Mechanical hand drill

- Drill bits (.8mm & 1mm)
- Hacksaw
- Sand paper
- Paint or permanent ink
- Copper clad board
- Ferric chloride solution

The different steps involved in the fabrication process are:

Designing of PCB

In the project work we need a printed circuit board for pcb manufacturing. It starts with drawing on copper clad sheets either by hand or screen printing on the pcb.

Selection of PCB

Paper phenolic is preferred material for common applications because it is very cheap and reliable. For professional stability and reliability pcb epoxy glass is the suitable material. The thickness of the copper clad sheet is specified according to the current carrying capacity of the circuit.

Etching

It is the process of removing unwanted copper from the processed board using etching solutions. In order to do this, the pcb is dipped into the etching solution which is ferric chloride solution. Once the unwanted copper has been displaced into the solution the pcb is taken out and dried.

Drilling

The holes of mounting components are drilled using a mechanical hand drill. The holes of IC pins are drilled with .8mm drill bit and all other holes are drilled with 1mm drill bit.

COMPONENTS LIST

COMPONENTS	SPECIFICATION	QUANTITY
DTMF RECEIVER IC	HT9170	1
DECODER IC	LS7447	1
7 SEGMENT DISPLAY	LTS 542	1
OR GATE	IC 7432	1
TONE GENERATOR	UM66	1

TRANSISTOR	BC 548 2N2222	
CRYSTAL	3.578MHz	1
ZENER DIODE	3.3V.5W	1
DIODE	1N4001	1
LED		1
INHIBIT SWITCH		
SPEAKER	4Ω, .5 W	1
CAPACITOR	.1UF	2
RESISTORS		

CONCLUSION

We were successful in completing the project of **"Telephone Operated Calling System".** It was a wonderful experience as we attained the basic knowledge on different steps in circuit manufacturing such as PCB fabrication, soldering components, circuit testing and debugging which will surely help us in our career in electronics field.

BIBLOGRAPHY

1. Electronics for You (Magazine)
2. www.alldatasheets.com
3. www.datasheetcatalog.com
4. Circuit Designer (Software)

7447 - BCD to 7-Segment Decoder/Driver with (15V) Open Collector Output

Pin Layout

LI-
CE'
I-

mi
till
LI¥

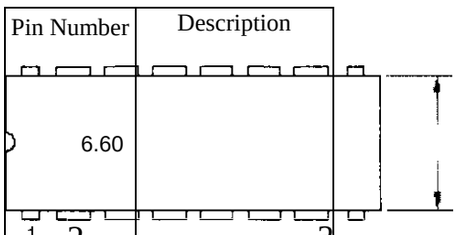
74-47
BCD ta 7-Seqment
Decoder/Driver wiih (15V)
Open Collector Ouiput

Features

i----------
I ►Output Drive Capability -10 LSTTL Loads
►Outputs Directly Interface to CMOS, NMOS and TTL
| ►large Operating Voltage Range I
►Low Input Current ►High Noise Immunity

in Description,

Pin Number	Description
1	BCD B Input
2	BCD C Input
3	Lamp Test
4	RB Output
5	RB Input
6	BCD D Input
7	BCD A Input



i
o

1615 14 13 12 1110
9

g	Ground	l§I5.Hill21110 9
9	7-Segment e Output	p
10	7-Segment d Output	6 DU 11
11	7-Segment c Output	1 2 3 4 5 6 7 8
12	7-Segment b Output	---------- 19.94 ----------
13	7-Segment a Output	nnnnnnrm
14	7-Segment g Output	2,54
15	7-Segment f Output	
16	Positive Supply	16-Pin DIP

hnical Data

jlol	LOW Level Output Current				16 mA	|
Ta	Free Air Operating Temperature | 0				"WT^ o c i	
Electrical Characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Vi	Input Clamp	vCC=Min,Ii=-12mA Voltage			-1.5	V
Voh	HIGH Level Output Voltage	Vcc=Min,**Ioh**=MAX,Vil=MAX	2.4	3.4		V
Vol	LOW Level Output Voltage	Vcc=Min,Iol=MAX,Vih=MAX		0.2	0.4	V
Ii	Input Current@MAX Input Voltage	Vcc=Max,Vi=5.5V			1	mA
Iih	HIGH Level Input	Vcc=Max,Vi=2.4V			40	uA

	Current					
Iil	LOW Level Input Current	Vcc=Max,Vi=0.4V			-1.6	mA
los	Short Circuit Output Current	Vcc=Max	-18		-55	mA
lech	Supply Current with Outputs HIGH	Vcc=Max		4	8	mA
Iccl	Supply Current with Outputs LOW	Vcc=Max		12	22	mA

Switching Characteristics
at Vcc=5V,Ta=25oC

Symbol	Parameter	Conditions	Min	Max	Units
tplh	Propogation Delay Time LOW-to-HIGH Level Output	Cl=15pF R1=400R		22	nS
,tphl	Propogation Delay Time HIGH-to-LOW Level Output			15	nS

HOLTEK

HT9170 DTMF Receiver

Features

Operating voltage: 2.5V-5.5V
Minimal external components
No external filter is required
Low standby current (on power down mode)
Excellent performance

Tristate data output for ***iC** interface 3.58MHz crystal or ceramic resonator 1633Hz can be inhibited by the INH pin HT9170B: 18-pin DIP package HT9170D: 18-pin SOP package

General Description

The HT9170 series are Dual Tone Multi Frequency (DTMF) receivers integrated with digital decoder and bandsplit filter functions. The HT9170B and HT9170D types supply power-down mode and inhibit mode operations. All types of the HT9170 series use digital counting techniques to detect and decode all the 16 DTMF tone pairs into a 4-bit code output.

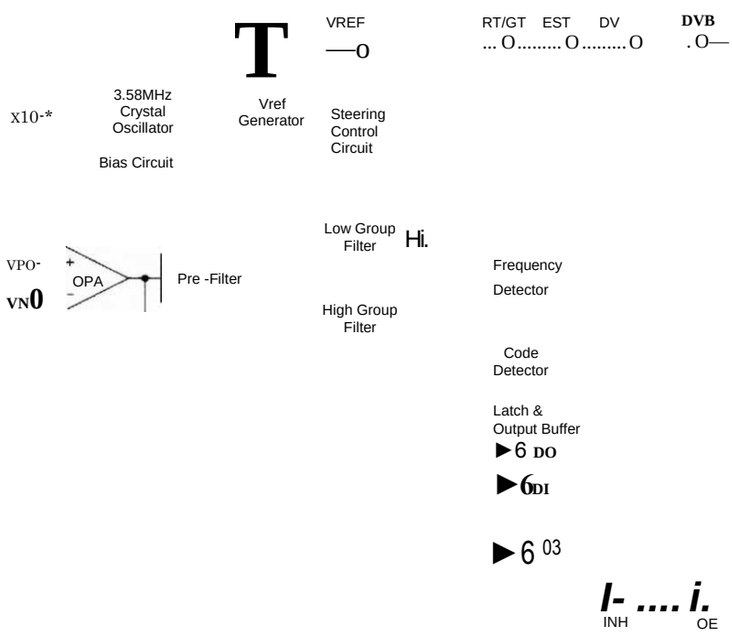
Highly accurate switched capacitor filters are employed to divide tone (DTMF) signals into low and high group signals. A built-in dial tone rejection circuit is provided to eliminate the need for pre-filtering.

Selection Table

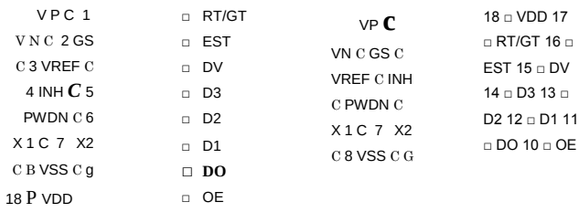
^Function Part No.\	Operating Voltage	osc Frequency	Tristate Data Output	Power Down	1633Hz Inhibit	DV	DVB	Package
HT9170B	2.5V-5.5V	3.58MHz	V	V	V	V	—	18 DIP
HT9170D	2.5V-5.5V	3.58MHz	V		V	V	—	18 SOP

December 20, 1999

Block Diagram



Pin Assignment



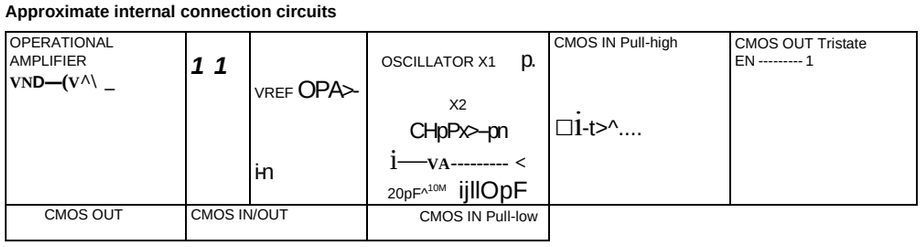
HT9170B - 18 DIP

HT9170D - 18 SOP

Pin Description

Pin Name	I/O	Internal Connection	Description
VP	I	OPERATIONAL AMPLIFIER	Operational amplifier non-inverting input
VN	I		Operational amplifier inverting input
GS	0		Operational amplifier output terminal
VREF	0	VREF	Reference voltage output, normally $V_{DD}/2$
XI	I	OSCILLATOR	The system oscillator consists of an inverter, a bias resistor and the necessary load capacitor on chip. A standard 3.579545MHz crystal connected to XI and X2 terminals implements the oscillator function.
X2	0		
PWDN	I	CMOS IN Pull-low	Active high. This enables the device to go into power down mode and inhibits the oscillator. This pin input is internally pulled down.
INH	I	CMOS IN Pull-low	Logic high. This inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
VSS	—	—	Negative power supply
OE	I	CMOS IN Pull-high	D0-D3 output enable, high active
D0-D3	0	CMOS OUT Tristate	Receiving data output terminals OE="H": Output enable OE="L": High impedance
DV	0	CMOS OUT	Data valid output When the chip receives a valid tone (DTMF) signal, the DV goes high; otherwise it remains low.
EST	0	CMOS OUT	Early steering output (see Functional Description)
RT/GT	I/O	CMOS IN/OUT	Tone acquisition time and release time can be set through connection with external resistor and capacitor.
VDD	—		Positive power supply, 2.5V-5.5V for normal operation
DVB	0	CMOS OUT	One-shot type data valid output, normal high, when the chip receives a valid time (DTMF) signal, the DVB goes low for 10ms.

Approximate internal connection circuits



Absolute Maximum Ratings

Supply Voltage .....-0.3V to 6V Storage Temperature.....-50°C to 125°C

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V Operating Temperature..... -20°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.5	5	5.5	V
I_{DD}	Operating Current	5V	—	—	3.0	7	mA
I_{STB}	Standby Current	5V	PWDN=5V	—	10	25	uA
VIL	"Low" Input Voltage	5V	—	—	—	1.0	V
Vm	"High" Input Voltage	5V	—	4.0	—	—	V

In,	"Low" Input Current	5V	VVP=VVN=0V	—	—	0.1	uA
Ira	"High" Input Current	5V	VVP=VVN=5V	—	—	0.1	UA
ROE	Pull-high Resistance (OE)	5V	V_{OE}=0V	60	100	150	ko
R_{IN}	Input Impedance (VN, VP)	5V	—	—	10	—	Mn

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Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
IfJH	Source Current (D0-D3, EST, DV)	5V	V_{OUT}=4.5V	-0.4	-0.8	—	mA
IOL	Sink Current (D0-D3, EST, DV)	5V	V_{OUT}=0.5V	1.0	2.5	—	mA
fosc	System Frequency	5V	Crystal=3.5795MHz	3.5759	3.5795	3.5831	MHz

A.C. Characteristics

f_{0SC}=3.5795MHz, Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
DTMF Signal							
	Input Signal Level	3V		-36	—	-6	dBm
		5V		-29	—	1	
	Twist Accept Limit (Positive)	5V		—	10	—	dB
	Twist Accept Limit (Negative)	5V		—	10	—	dB
	■Dial Tone Tolerance	5V		—	18	—	dB
	Noise Tolerance	5V		—	-12	—	dB
	Third Tone Tolerance	5V		—	-16	—	dB
	Frequency Deviation Acceptance	5V		—	—	±1.5	%
	Frequency Deviation Rejection	5V		±3.5	—	—	%
	Power Up Time **(tprj)** (See Figure 4.)	5V		—	30	—	ms
Gain Setting Amplifier							
RTN	Input Resistance	5V	—	—	10	—	MO.
!IN	Input Leakage Current	5V	VSS<(VVP,VVN)<VDD	—	0.1	—	uA
Vos	Offset Voltage	5V	—	—	+25	—	mV
PsRR	Power Supply Rejection	5V	100 Hz	—	60	—	dB
CMRR	Common Mode Rejection	5V	-3V<V_{IN}<3V	—	60	—	dB
$A_{V}o$	Open Loop Gain	5V		—	65	—	dB
f_T	Gain Band Width	5V	—	—	1.5	—	MHz
VOUT	Output Voltage Swing	5V	R_L>100kn	—	4.5	—	VPP

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
RL	Load Resistance (GS)	5V	—	—	50	—	kfi
CL	Load Capacitance (GS)	5V	—	—	100	—	pF
V_{CM}	Common Mode Range	5V	No load	—	3.0	—	**VPP**
Steering Control							
tDP	Tone Present Detection Time			5	16	22	ms
	Tone Absent Detection Time			—	4	8.5	ms
Ucc	Acceptable Tone Duration			—	—	42	ms
tREJ	Rejected Tone Duration			20	—	—	ms
tlA	Acceptable Inter-**digit** Pause			—	—	42	ms
tm	Rejected Inter-digit Pause			20	—	—	ms
tpDO	Propagation Delay (RT/**GT** to DO)			—	8	11	us
tpDV	Propagation Delay (RT/GT to DV)			—	12	—	us
tDOV.	Output Data Set Up (DO to DV)			—	4.5	—	us
tDDO	Disable Delay (OE to DO)			—	300	—	ns
tEDO	Enable Delay (OE to DO)			—	50	60	ns

Note: DO=D0~D3

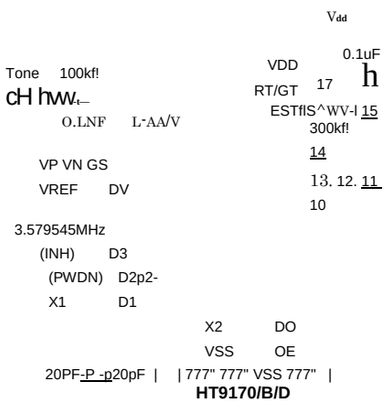

Figure 1. Test circuit

Functional Description

Overview

The HT9170 series tone decoders consist of three band pass filters and two digital decode circuits to convert a tone (DTMF) signal into digital code output.

An operational amplifier is built-in to adjust the input signal (refer to Figure 2).

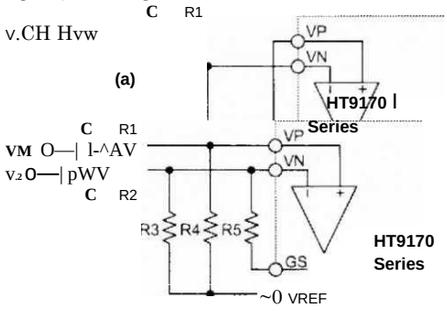

Figure 2. Input operation for amplifier application circuits

Standard input circuit
(b) Differential input circuit

The pre-filter is a band rejection filter which reduces the dialing tone from 350Hz to 400Hz.

The low group filter filters low group frequency signal output whereas the high group filter filters high group frequency signal output.

Each filter output is followed by a zero-crossing detector with hysteresis. When each signal amplitude at the output exceeds the specified level, it is transferred to full swing logic signal.

When input signals are recognized to be effective, DV becomes high, and the correct tone code (DTMF) digit is transferred.

Steering control circuit

The steering control circuit is used for measuring the effective signal duration and for protecting against drop out of valid signals. It employs the analog delay by external RC time-constant controlled by EST.

The timing is shown in Figure 3. The EST pin is normally low and draws the RT/GT pin to keep low through discharge of external RC. When a valid tone input is detected, EST goes high to charge RT/GT through RC.

When the voltage of RT/GT changes from 0 to V_{XRT} (2.35V for 5V supply), the input signal is effective, and the correct code will be created by the code detector. After D0-D3 are completely latched, DV output becomes high. When the voltage of RT/GT falls down from VDD to V_{TRT} (i.e.., when there is no input tone), DV output becomes low, and D0-D3 keeps data until a next valid tone input is produced.

By selecting adequate external RC value, the minimum acceptable input tone duration (t^cc) and the minimum acceptable inter-tone rejection (tr^) can be set. External components (R, C) are chosen by the formula (refer to Figure 5.):

tACC=tDP+tGTP;

tIR=tDA+tGTA;

where t^cc[1] Tone duration acceptable time

top: EST output delay time ("L"->"H") **tQTP**:

Tone present time tiR: Inter-digit pause

rejection time tnA: EST output delay time

("H"->"L") **tcTA**: Tone absent time